

## **AMENDMENTS TO THE SPECIFICATION**

**Please delete paragraph [0023], and replace it with the following new paragraph:**

[0023] On the other hand, when the NMOS transistor MN1 is used, a gate-drain voltage difference Vgd2 of the NMOS transistor MN2 is the maximum IVC voltage (when IVC is lower than EVC), as shown in FIG. 2. When the IVC is equivalent to the EVC, the gate-drain voltage difference Vgd2 of the NMOS MN2 is IVC-Vtnh. In other words, an electric field applied to the gate insulation layer of the NMOS transistor MN2 may be alleviated. Therefore, the NMOS transistor MN1 may be used as an interface (or for attenuating an electric field) and may be arranged between the internal circuits 12 and 14. NMOS transistor ~~NM1~~MN1 prevents the gate insulation layer of the NMOS transistor MN2 from being broken by applying a high voltage to the drain of NMOS transistor MN2, as well as to prevent any lowering of the turn-on speed of the NMOS transistor MN2.

**Please delete paragraph [0028], and replace it with the following new paragraph:**

[0028] Referring again to FIG. 3, in operation, when an input signal IN1 is at a low level of ground voltage VSS and at least one of input signals IN2-IN5 is at a low level of a ground voltage VSS, internal node ND1 may be precharged to high voltage VPP through PMOS transistor MP2. In this case, the output signal OUT becomes a low level of the ground voltage VSS, so that PMOS transistor ~~MP2~~MP3 is also turned on. Since the gate of NMOS transistor MN4 (coupled to an internal power supply voltage IVC or an external power supply voltage EVC) is always in a turn-on state, a voltage of IVC-Vtnl is applied to the drain of NMOS transistor MN4 through NMOS transistor MN3. That is, a voltage applied to the drain of the NMOS transistor MN4 is restricted by NMOS transistor MN3 of the interface circuit 26. Accordingly, although NMOS transistor MN4 has a relatively thin gate insulation layer, the gate

insulation layer of the NMOS transistor MN4 is not broken by the high voltage VPP, and a turn-on speed of NMOS transistor NM4 does not need to be lowered. Similarly, since IVC/EVC is always applied to the gate of the NMOS transistor MN3, a gate-drain voltage difference of NMOS transistor MN3 is VPP-IVC/EVC. Although NMOS transistor MN3 has a relatively thin gate insulation layer, the gate insulation layer of the NMOS transistor MN3 is not broken by the high voltage VPP.

**Please delete paragraph [0032], and replace it with the following new paragraph:**

[0032] In operation, when an input signal IN is at a low level, NMOS transistor MN11 is turned off and MOS transistor MN12 is turned on. Since the ND3 node goes to a low level through NMOS transistors MN10 and MN12, PMOS transistor MP5 is turned on and an output signal goes to a high level of high voltage VPP. When the input signal is at a high level, the NMOS transistor MN13MN12 is turned off and the NMOS transistor MN11 is turned on. Since the ND2 node goes to a low level through NMOS transistors MN9 and MN11, the PMOS transistor MP6 is turned on and an output signal OUT goes to a low level of ground voltage VSS.

**Please delete paragraph [0038], and replace it with the following new paragraph:**

[0038] The level shift blocks and the row decoder and driving blocks according to the exemplary embodiments of the present invention may be implemented using a dual circuit device of a dual insulation system, as described in any of FIG. 1, FIG. 3 and FIG. 4, for example. As shown in FIG. 5, outputsoutput signals of the respective level shift blocks may only be input to corresponding memory blocks, in an effort to reduce power consumption.

**Please delete paragraph [0046], and replace it with the following new paragraph:**

[0046] Referring to FIG. 7, the row decoder and driver circuit 131 may include PMOS transistors MP22, MP23 and MP24 and NMOS transistors MN24, MN25, MN26 and MN27. PMOS transistor MP22 has a gate connected to receive a control signal P\_0, a source coupled to a high voltage VPP, and a drain coupled to an internal node ND22. The NMOS transistors MN24-MN26 may be serially coupled between the internal node ND24ND22 and a ground voltage VSS, and are controlled by corresponding decoding signals DRA0k0, DRAi0, and DRAj0. PMOS transistor MP23 has a gate coupled to an output terminal ND24, a source coupled to a high voltage VPP, and a drain coupled to an internal node ND23ND22. PMOS transistor MP24 and NMOS transistor MN27 may constitute an inverter, and are coupled between the internal node ND22 and the output terminal ND24 (i.e., a word line WL).

**Please delete paragraph [0048], and replace it with the following new paragraph:**

[0048] When the control signal P\_0 has a high level of a high voltage VPP and all decoding signals DRA0k0, DRAi0DRAj0, and DRAj0 are at a high level, a current path between the high voltage VPP and the internal node ND22 is open while a current path is formed between the internal node ND22 and the ground voltage VSS. Accordingly, the word line WL is driven with the high voltage VPP through PMOS transistor MP24. Since the high voltage VPP of node ND22 is transmitted through NMOS transistor MN24 (serving as an interface or voltage restricting means), a gate insulation layer of the NMOS transistor MN27 is not affected by the high voltage VPP.

**Please delete paragraph [0056], and replace it with the following new paragraph:**

[0056] The row decoder and driver circuit 131' may include PMOS transistor P25MP25, MP26 and MP27 and the NMOS transistors MN28, MN29, MN30, MN31, MN32 and MN33. Each of the

transistors MP25, MP26, MP27 and MN33 may have a relatively thick gate insulation layer. Each of the transistors MN28-MN32 may have a relatively thin gate insulation layer. PMOS transistors MP25 and MP26 may constitute a first internal circuit operating with a high voltage VPP, and NMOS transistors MN29-MN32 may constitute a second internal circuit operating with an internal power supply voltage IVC or an external power supply voltage EVC. The NMOS transistor MN28 may act as an interface circuit (or voltage restricting means) for restricting a voltage applied from the first internal circuit to the second internal circuit. The row decoder and driver circuit of FIG. 10 operates the same as the integrated circuit device of FIG. 3, thus operation will not be explained in further detail.